Amendments to the Claims

1. (*Currently Amended*) A semiconductor device comprising a carrier with a first and a second side situated opposite to each other, which carrier has a first electroconductive layer on the first side, which electroconductive layer is patterned in accordance with a desired pattern, thereby defining a number of mutually isolated connection conductors,

[[-]] on which first side of the carrier a semiconductor element is present, which semiconductor element is provided with connection regions that are electroconductively connected via connection means with the connection conductors of the carrier, which semiconductor element is encapsulated in a passivating envelope that extends as far as the carrier,

[[-]] on which second side, contact surfaces are defined in the connection conductors for placement on a substrate,

characterized in that the envelope is mechanically anchored in the connection conductors, for which purpose the connection conductors are provided with side faces having recesses.

2. (*Original*) A semiconductor device as claimed in claim 1, characterized in that, in addition to the first layer, the carrier comprises a second layer and a third layer, the second layer comprising a material that can be etched in an etchant that leaves the first and the third layer substantially in tact.

3. (*Currently Amended*) A semiconductor device as claimed in claim 1, ~~claim 1 or 2,~~ characterized in that the apertures extend as far as the second side of the carrier.

4. (*Original*) A semiconductor device as claimed in claim 1, characterized in that the connection means are bumps, which bumps are also used to attach the semiconductor element onto the carrier.

5. (*Original*) A semiconductor device as claimed in claim 2, characterized in that the first and the third layer contain copper, and the second layer contains a material selected from the group composed of Al and Ni-Fe.

6. (*Currently Amended*) A semiconductor device as claimed in claim 1, ~~claim 1 or 2,~~ characterized in that the carrier comprises a number of electrically insulating and conductive layers, at least one passive component being embedded in said layers.

7. (*Original*) A method of manufacturing a carrier having a first and a second side situated opposite to each other, which carrier comprises, on the first side, a first electroconductive layer that is patterned in accordance with a desired pattern, thereby defining a number of mutually isolated connection conductors, which carrier further comprises a second and a third layer,

characterized in that the second layer is etched in an etchant that leaves the first layer and the third layer substantially in tact, said etching leading to underetching of the first layer, resulting in the formation of recesses in the connection conductors.

8. (*Original*) A method as claimed in claim 7, characterized in that the pattern is defined by means of punching, apertures being formed that extend from the first side to the second side of the carrier, and the connection conductors remaining connected to a framework in the carrier by means of leads.

9. (*Currently Amended*) A method as claimed in claim 7, characterized in that:

[[-]] the carrier is provided with an etch mask on the second side, which etch mask is resistant to a heat treatment;

[[-]] the first layer is patterned by means of etching, and

[[-]] the mechanical strength of the third layer is sufficient, so that the carrier formed does not disintegrate and has an electroconductive surface on the second side.

10. (*Currently Amended*) A method of manufacturing a number of semiconductor devices comprising a semiconductor element that is provided with connection regions, which method comprises the following steps:

[[-]] providing the semiconductor element on the first side of the carrier that can be obtained by using the method as claimed in any one of the claims 7-9, the connection means being used to establish an electroconductive connection between the connection regions and the connection conductors of the carrier;

[[-]] providing a passivating envelope such that the envelope extends into the recesses defined in the carrier; and

- separating the semiconductor devices.

11. (*Currently Amended*) A method as claimed in claim 10, characterized in that the carrier as claimed in claim 8 is used, wherein:

[[-]] conductive wires are used as connection means;

[[-]] the carrier is present on a substrate when the passivating envelope is provided; and

[[-]] in the separating process, the leads between the connection conductors and the framework are cut through.

12. (*Original*) A method as claimed in claim 10, characterized in that the carrier obtainable with the method as claimed in claim 9 is used, wherein, prior to separating, the second side of the carrier is treated with an etchant, thereby patterning the electroconductive surface of the third layer, after which the etch mask is removed.